This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1-9 (canceled)

10. (currently amended) A method for enabling a single pixel frame buffer for simultaneous rendering and display in a computer image generator, comprising the steps of:

(a) dividing a geometry buffer into a plurality of screen bins;

(b) storing primitives in each screen bin the primitives touch;

(c) rendering the screen bins by row from top to bottom, into the single pixel frame buffer;

(d) displaying at least one row of screen bins rendered before the rendering of all the screen bins has completed, wherein the displaying of the screen bins takes place after a selected portion of the screen bins for a current field have been rendered.

11. (original) A method as in claim 10 further comprising the step of reducing the transport delay without allowing the display step to overlap a rendering envelope.

12. (original) A method as in claim 10 further comprising the step of reducing the transport delay and allowing the display step to overlap a rendering envelope.

13. (original) A method as in claim 10 further comprising the step of rendering at least one row of screen bins before the display step begins.

14. (original) A method as in claim 10 further comprising the step of reducing the transport delay by allowing the display step to overlap a rendering envelope without allowing pixels from a previous field to be displayed.

15-23. (canceled)

24. (currently amended) A method for enabling a single pixel frame buffer for simultaneous rendering and display in a computer image generator, comprising the steps of:

(a) dividing a geometry buffer into a plurality of screen bins;

(b) storing primitives in each screen bin containing a portion of the primitive;

(c) rendering the screen bins, by row from top to bottom, into the single pixel frame buffer;

(d) displaying at least one rendered screen bin when the rendering of the screen bins for the single pixel frame buffer is at least ½ completed.

25. (canceled)

26. (previously presented) A method as in claim 24, further comprising the step of using a hardware interlock to ensure that the rendering step does not advance ahead of the display step.

27. (previously presented) A method as in claim 26, further comprising the step of using a row based hardware interlock to ensure that the rendering step does not advance ahead of the display step.

28. (previously presented) A method as in claim 24, further comprising the step of executing the rendering and displaying steps concurrently within the same frame buffer.

29. (previously presented) A method as in claim 24, wherein step (d) further comprises using an independent timer to control toggling of the geometry buffer.

30. (canceled)

31. (canceled)

32. (currently amended) An image generator with a single pixel frame buffer enabled for simultaneous rendering and display, comprising:

(a) a geometry buffer divided into a plurality of screen bins;

(b) a plurality of primitives, stored in all of the screen bins that touch a screen region defined by the screen bin;

(c) a rendering engine, configured to render the primitives in the screen bins into the single pixel frame buffer by row and from top to bottom;

(d) a display processor, configured to display at least one rendered screen bin on a display screen before the rendering engine has completed rendering all the screen bins;

(e) wherein the display processor begins to display the screen bins rendered when the rendering of the screen bins is at least ½ complete.

33. (canceled)

34. (currently amended) An image generator as in claim 32, further comprising a geometry engine configured to transform ~~the~~ a database and the plurality of primitives used by the image generator.

35. (currently amended) An image generator as in claim 32, further comprising a real-time controller configured to receive real-time control information and compute ~~the~~ transformation matrices.

36-38. (canceled)